REMARKS

Claims 65 and 68-103 are pending in this application. Claims 78 and 79 have been amended to correct claim dependency. Applicants note that claim 76 has been indicated as being allowable if "rewritten in independent form to include all of the limitations of the base claim and any intervening claims." (Office Action at 5). Accordingly, amended independent claim 76, which now incorporates all limitations of claim 65, is now in condition for allowance. Applicants also acknowledge with appreciation the allowance of claims 92-103.

Claims 65, 68, 69, 74, 75 and 84-88 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Raaijmakers et al. (U.S. Patent No. 6,780,704) ("Raaijmakers") in view of Wei et al. (U.S. Patent No. 6,046,084) ("Wei"). This rejection is respectfully traversed.

The claimed invention relates to a method of forming an MIS capacitor. As such, independent claim 65 recites a "method of forming an MIS capacitor" by *inter alia* "forming a semiconductive layer of hemispherical grained polysilicon over a substrate," "opening the grains which form said layer of hemispherical grained polysilicon to activate said grains" and "forming a dielectric layer comprising aluminum oxide over said semiconductive layer by atomic layer deposition." Independent claim 65 also recites "forming a metal nitride layer over said dielectric layer."

Raaijmakers relates to "conformal capacitor dielectrics over textured silicon electrodes for integrated memory cells." (Abstract). Raaijmakers teaches that "[T]he first electrodes include hemispherical grain (HSG) silicon for increasing the capacitor

plate surface area" and that "[T]he HSG topography is then exposed to alternating chemistries to form monolayers of a desired dielectric material." (Abstract).

Wei relates to a "process for creating a storage node structure, for a DRAM capacitor structure, featuring increased storage node surface area, via use of an HSG silicon layer, on an underlying storage node shape." (Abstract). According to Wei, "[T]he process features the use of an isotropic, buffered HF etch procedure, applied to the HSG silicon layer, to increase the space between the concave and convex features, of the HSG silicon layer." (Abstract).

The subject matter of claims 65, 68, 69, 74, 75 and 84-88 would not have been obvious over Raaijmakers in view of Wei. Specifically, the Office Action fails to establish a *prima facie* case of obviousness. Applicants note that courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

In the present case, neither Raaijmakers nor Wei, whether considered alone or in combination, teaches or suggests all limitations of independent claim 65. Neither Raaijmakers nor Wei teaches or suggests "forming a semiconductive layer of hemispherical grained polysilicon over a substrate," "opening the grains which form said layer of hemispherical grained polysilicon to activate said grains" and "forming a dielectric layer comprising aluminum oxide over said semiconductive layer by atomic

layer deposition," as independent claim 65 recites. Raaijmakers teaches only that "[I]f necessary, the exposed surfaces of the bottom electrode (e.g., the HSG silicon of the preferred embodiments) are terminated . . . to react with the first phase of the ALD process." (Col. 8, lines 56-59). Raaijmakers fails to disclose, teach or suggest, however, "opening the grains which form said layer of hemispherical grained polysilicon to activate said grains," much less "opening the grains which form said layer of hemispherical grained polysilicon to activate said grains" and "forming a dielectric layer comprising aluminum oxide over said semiconductive layer by atomic layer deposition," as in the claimed invention.

Similarly, Wei teaches that an HSG silicon seed layer is formed over an "amorphous silicon, or a polysilicon layer . . . at a thickness between about 400 to 600 Angstroms" and that an "ONO, (Oxidized--silicon Nitride--silicon Oxide), layer 14" is formed on the HSG layer. (Col. 4, lines 35-55; Col. 5, lines 27-30). Wei does not disclose, teach or suggest, however, "opening the grains which form said layer of hemispherical grained polysilicon to activate said grains" or "forming a dielectric layer comprising aluminum oxide over said semiconductive layer by atomic layer deposition," much less "opening the grains which form said layer of hemispherical grained polysilicon to activate said grains," "forming a dielectric layer comprising aluminum oxide over said semiconductive layer by atomic layer deposition," and "forming a metal nitride layer over said dielectric layer," as claim 65 recites.

In addition, Applicants note that a person of ordinary skill in the art would not have been motivated to combine the teachings of Raaijmakers with those of Wei, as the Office Action asserts. The crux of Raaijmakers is a method "of increasing the dielectric constant (k) of the capacitor dielectric" by providing "uniformly thick dielectric layers" by "alternating reactant phases, wherein each phase has a self-limiting

effect." (Col. 4, lines 53-64). In this manner, Raaijmakers teaches a specific process for the formation of dielectric layers from "[M]etal oxides and ternary materials having dielectric constants of greater than about 10 . . . formed by alternately adsorbing self-terminated metal or silicon complex monolayers through ligand-exchange reactions." (Col. 4, lines 64-67).

On the other hand, the crux of Wei is the formation of an HSG layer over a lower capacitor electrode to improve the quality of an overlying dielectric layer. Wei specifically teaches that an "ONO, (Oxidized--silicon Nitride--silicon Oxide), layer 14" is formed on the HSG layer. (Col. 4, lines 35-55; Col. 5, lines 27-30). Thus, a person of ordinary skill in the art would not have been motivated to combine Raaijmakers, which teaches a specific process for the formation of dielectric layers from "[M]etal oxides and ternary materials having dielectric constants of greater than about 10," with Wei, which teaches the formation of an "ONO, (Oxidized--silicon Nitride--silicon Oxide), layer." For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness and withdrawal of the rejection of claims 65, 68, 69, 74, 75 and 84-88 is respectfully requested.

Claims 71 and 72 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Raaijmakers in view of Wei and further in view of Lin et al. (U.S. Patent No. 6,165,830) ("Lin"). This rejection is respectfully traversed.

Claims 71 and 72 recite "subjecting said layer of hemispherical grained polysilicon to an anneal process" and "subjecting said layer of hemispherical grained polysilicon to a PH_3 anneal," respectively.

Lin teaches "the use of an HSG silicon layer, on a doped amorphous silicon, storage node shape, with the HSG silicon layer supplying increased surface area, and

thus increased capacitance, for the DRAM capacitor." (Abstract). According to Lin, a "doped polysilicon layer, selectively deposited on the underlying HSG silicon layer, supplies additional dopant to the HSG silicon layer, residing on the doped amorphous silicon, storage node shape, thus minimizing a capacitance depletion phenomena, that can be present with lightly doped storage node structures." (Abstract).

The subject matter of claims 71 and 72 would not have been obvious over Raaijmakers, Wei and Lin, whether considered alone or in combination. The Office Action fails again to establish a *prima facie* case of obviousness. None of Raaijmakers, Wei and Lin, alone or in combination, discloses, teaches or suggests "opening the grains which form said layer of hemispherical grained polysilicon to activate said grains," much less "opening the grains which form said layer of hemispherical grained polysilicon to activate said grains" and "forming a dielectric layer comprising aluminum oxide over said semiconductive layer by atomic layer deposition," as independent claim 65 recites.

Applicants also note that a person of ordinary skill in the art would not have been motivated to combine the teachings of Lin with those of Raaijmakers and Lin, as the Office Action asserts. The crux of Lin is a method of doping an HSG layer via a selective deposition of a doped polysilicon layer. (Col. 1, lines 52-55). In contrast, Raaijmakers teaches a specific process for the formation of dielectric layers from "[M]etal oxides and ternary materials having dielectric constants of greater than about 10 . . . formed by alternately adsorbing self-terminated metal or silicon complex monolayers through ligand-exchange reactions" (Col. 4, lines 64-67), while Wei teaches that an "ONO, (Oxidized--silicon Nitride--silicon Oxide), layer 14" is formed on the HSG layer. (Col. 4, lines 35-55; Col. 5, lines 27-30). Thus, a person of ordinary skill in the art would not have been motivated to combine Lin (which teaches doping an HSG

layer via a selective deposition of a doped polysilicon layer) with Raaijmakers (which teaches a specific process for the formation of dielectric layers from "[M]etal oxides and ternary materials having dielectric constants of greater than about 10") and further with Wei (which teaches the formation of an "ONO, (Oxidized--silicon Nitride--silicon Oxide), layer"). For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness and withdrawal of the rejection of claims 71 and 72 is also respectfully requested.

Allowance of all pending claims is solicited.

Dated: August 24, 2005

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Gabriela I. Coman
Registration No.: 50,515
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicants